QP Co	de: D 123107	Total Pages:	2		Name:	
					Register No.	
	SECOND SEMESTER			XAMIN	IATION, APRIL 2025	
	ELEGRANIA DA LEUR	ELECTROI		TAL FL	CTRONICC	
	ELE2MN101 – FUN	1DAMENTALS (ECTRONICS	
Maxim	num Time :2 Hours	724 Admission	Onware		Maximum Marks :70	
		Section	4			
	All Questions can be answered	. Each Questic	n carrie	es 3 ma	arks (Ceiling : 24 Marks)	
1	Convert the hexadecimal number ABA2 to decimal number and binary number.					
2	Draw the symbol of (i) XNOR and (ii) OR. Give the truth tables also.					
3	Implement the XOR gate using NAND gates only.					
4	Explain DeMorgan's Theorems.					
5	Express the following Boolean expression into standard POS form. $F = (A+C)(B'+C)(A'+B)$					
5	What is a decoder? Explain.					
7	What is the difference between edge triggering and pulse triggering?					
8	Draw the logic diagram of Johnson's counter.					
9	Write a note on multiplexers.					
10	Differentiate volatile and non-volatile memory.					
		Section I	3			
	All Questions can be answered	. Each Questic	on carrie	es 6 ma	arks (Ceiling : 36 Marks)	
11	Simplify the given expression using Boolean Algebra. F(A,B,C)=A'B'C+A'BC'+ABC'+ABC					
12	Design a full adder and realize using logics gates.					
13	Draw the logic circuit of a 1:4 demultiplexer. Explain its operation.					
14	Draw the logic circuit of serial in serial out shift register and explain its operation.					
15	Explain the logic circuit of 2-bit synchronous counter.					
16	Explain a single RAM cell with a logic diagram.					
17	Explain the write operation in a single bit memory.					
438	What are the different types of	ROM? Explain.				

Section C					
Answer any ONE .Each Question carries 10 marks (1x10=10 Marks)					
19	Minimize the following function using Karnaugh map.				
	f (A, B, C, D) = Σ m (0, 1, 5, 7, 8, 9, 13, 15)				
20	What is a flip flop? Explain SR and D flip flops with the logic diagram and truth table.				

