D 72945 (Pages : 2) Name.....

Reg. No.....

FIRST SEMESTER M.A./M.Sc./M.Com. DEGREE EXAMINATION DECEMBER 2019

(CBCSS)

Computer Science

CSS 1C 05—COMPUTER ORGANIZATION AND ARCHITECTURE

(2019 Admissions)

Time : Three Hours Maximum : 30 Weightage

Section A

Answer any **four** *questions.*
Each question carries 2 *weightage.*

1. Draw block diagram and explain the working of Full Adder.
2. Explain the working of SR Flip Flop.
3. Explain the concept of instruction cycle.
4. Differentiate between hardwired controland microprogrammed control.
5. Explain floating point number representation.
6. Explain memory interleaving.
7. List and explain any *four* addressing modes.

(4 × 2 = 8 weightage)

Section B

Answer any **four** *questions.*
Each question carries 3 *weightage.*

8. Simplify using K-map : F (P, Q, R, S) = Σ (0, 2, 5, 7, 8, 10, 13, 15).
9. Explain single bus and two bus organization.
10. With block diagram, explain sequential multiplier.
11. Explain cache memory organization and mapping (any *one* approach).
12. Write a note on Programmable Interrupt Controller.
13. Discuss the features of 8051 Micro controller.
14. Give and explain two examples each for arithmetic, logical, branching and data transfer instructions in 8085.

(4 × 3 = 12 weightage)

Turn over

Section C

Answer any **two** *questions.*
Each question carries 5 *weightage.*

15. Draw block diagram and explain the working of 4-bit binary counter.

16. Illustrate Booth's algorithm with suitable example.

17. Explain organization and operations of DMA mechanism.

18. Discuss 8086 architecture.

(2 × 5 = 10 weightage)